Bonded Substrates for Optoelectronic Applications

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Abstract

Bonded hydrophilic (SOI) and hydrophobic wafer pairs are applied as substrates for optical devices (pin-diodes and complex MOEMS). Important parameters of diodes are analysed at temperatures up to 160°C (dark current, photocurrent, CV-curves, rise time). Diodes produced especially on bonded hydrophobic wafer pairs show a similar or better behaviour than components prepared on the standard epitaxial wafers.

Keywords: wafer bonding, SOI wafer, MOEMS

1   Introduction

A fast growing market is expected for optical micro-electromechanical systems (MOEMS). MOEMS, are used in a wide range of applications where communication networks will be of major interest (1). The applications require the on chip integration of different functions including sensing, acting, and signal processing elements. Different functions, however, make it necessary to combine different materials to form heterogeneous substrates. The simplest one is a combination of two silicon materials of different doping type and level, respectively, to form epitaxial wafers, or SOI wafers (silicon-on-insulator), where a thin single-crystalline silicon layer is formed on an oxide layer grown on a silicon substrate. Silicon-based elements are widely used for optoelectronic applications in the visible and near-infrared region (2). The basic structure, e.g. of a Si photodetector, is a reverse biased pn-junction with an intermediate intrinsic layer (pin-diode). In this operation mode the space charge region is extended over the whole intrinsic layer (I-layer). Their thickness and quality strongly influence the efficiency of the diode. Most of today´s photodetectors are prepared on epitaxial wafers where an intrinsic layer was grown on a higher doped silicon substrate of the same type. The epitaxy process, however, limits the layer thickness to about 50 µm and the resistivity to less than about 500 Ωcm. In order to increase the efficiency of the photodetectors thicker (epitaxial) layers are required having also a lower sheet resistivity. Such layers can be prepared by semiconductor wafer direct bonding of silicon wafers having hydrophobic surfaces and a subsequent thinning to the required thickness. Furthermore, SOI wafers prepared by hydrophilic wafer bonding could be alternative substrates especially for high-speed optical communication devices or for high-

temperature applications (2,3). The present paper deals with the application of different wafer direct bonding techniques and the analysis of different Si/Si combinations to the preparation of single pin-diodes and of complex MOEMS. An optical distance sensor (ODS) is used for demonstration which is designed as an on-chip solution integrating the light source (e.g. a LED, incorporated into the silicon basis), the detecting element and the logic circuit.

2   Experimental

A CMOS process typically used for the preparation of the low-capacity and high-speed single photodiode SFD3.7 was applied (4). The diode is characterized by their large spectral response range (400 – 1100 nm), the low dark current (I_d = 150 pA at T = 300K), and the low rise time of 4.7 ns. The standard material for the production process acts as reference (epitaxial wafers having an n⁻-layer (about 500 Ωcm) on an n-type substrate (ρ = 10 – 20 Ωcm, diameter 4 in.). The diodes posses an island-like structure produced by deep-trench etching in order to suppress the cross-talking in diode arrays. Front side contacts are used.

Czochralski-grown (CZ) silicon wafers (diameter 4 in., (100) orientation, n-type, ρ = 10 – 20 Ωcm) and high resistivity float-zone (FZ) wafers (diameter 4 in., (100) orientation, n-type, ρ = 3 - 5 kΩcm) were used for the preparation of bonded wafer pairs. The CZ-grown wafer acts as substrate in all cases, while the FZ material is used as top layer. All wafers were initially cleaned in RCA 1,2 solutions. The wafers were bonded by using different pretreatments in order to make their surfaces hydrophobic or hydrophilic. For hydrophilic wafer bonding (SOI wafers) a 200 nm thick oxide layer was deposited on the substrate wafer by thermal LP-CVD. The bonding experiments were carried out at room temperature and with water flushing in a CL200 (Suess). After bonding the wafer pairs were

subsequently annealed at 1050°C for 4 hours in an oxygen atmosphere. After that the top wafers were thinned down by grinding and polishing (CMP) to thicknesses between 5 µm and 80 µm. The procedure is explained elsewhere (5,6).

Bonded hydrophobic wafer pairs were prepared by a SF_6/O_2 plasma treatment of the wafer surfaces instead of the generally used HF rinsing. The treatment in the SF_6/O_2 plasma causes an analogous surface structure as for HF dipping, i.e. a complete removing of the native oxide, but a bonding behaviour similar to hydrophilic bonded wafer pairs (7,8). Plasma treatments were carried out in an ALCATEL MCM 100 system (reactive ion etching at 13.56 MHz) using a $SF_6/18.9\%O_2$ plasma at a pressure of 1.4 Pa for 40 sec (rf power 80 W). The top wafers (FZ wafers) of the bonded and annealed samples were also thinned down to thicknesses between 5 µm and 80 µm. An analogous thinning procedure was applied as for SOI wafers.

The wafer pairs were analysed with respect to microscopic interface defects by infrared transmission microscopy immediately after bonding and annealing. The bonded wafer pairs were processed in the same CMOS runs as the epitaxial wafers. All diodes of the completely processed wafers were measured using the standard automatic test equipment. The results of the measurements of the dark current (I_d), the photocurrent (I_p), the rise time (t_r), and CV measurements are especially regarded for the interpretation. Furthermore, the temperature dependence of I_d was also measured on diodes separated and mounted in TO packages.

3 Results

Wafer Bonding: Bonding of hydrophilic wafers for SOI is a standard process. It should be noted, however, that the actual material combination of a FZ-silicon wafer and a CZ-silicon wafer is the reason for an increasing stress especially during the preparation of the SOI wafer (6). The mean reason for stress is the surface damage produced during grinding which, however, can be removed by an additional KOH etch step before the final polishing. For SOI wafers the breakdown voltage of the buried oxide (BOX) is most important. Breakdown voltages of more than $7 \cdot 10^7$ V/cm are measured at room temperature which corresponds to the general specification for SOI materials (9). On the other hand, the breakdown voltage drops only slightly if the measuring temperature increases to 150°C. The data also show that high breakdown voltages are obtained for different BOX layer thicknesses. In addition, the density of interface states is also reduced. Typical values of $9 \cdot 10^9$ cm^{-2} are obtained for this material.

Bonded hydrophobic wafer pairs were prepared by plasma treatments before bonding. A $SF_6/18.9\%O_2$ plasma was applied. The plasma treatment causes the removing of the oxide from the silicon surfaces. A

subsequent bonding of such surfaces result in a Si/Si interface without additional layers (10).

Characterization of pin-diodes: The general dependences of the dark current (I_d) and photocurrent (I_p) on the layer thickness, doping, and temperature were calculated (SPICE simulations) for design simulation of the photodiodes. The main results can be summarized as followed:

1. The dark current increases by a factor of about 1.5 if the layer thickness increases from 5 µm to 50 µm. Thicker layers does not change I_d because the space charge region is extended over the whole layer at a cutoff voltage of 2.5 V.
2. Increasing the temperature from room temperature to T = 200°C causes that the dark current increases about 4 orders of magnitude.
3. The dark current decreases as the dopant concentration of the layer increases.
4. The photocurrent increases with increasing thickness and doping of the layer.

The opposite behaviour of I_d and I_p causes that optimum parameters for the layer thickness and their doping concentration are needed. In addition, the large spectral range for application requires also a minimum thickness due to different carrier generation depths.

First electrical measurements were carried out on fully CMOS-processed wafers. Examples of bonded hydrophobic wafer pairs and SOI wafers are shown in Fig. 1 after device processing. Results of the measurements are summarized in Fig. 2. The dark current of individual pin-diodes prepared on the standard epitaxial material is about $9.5 \cdot 10^{-12}$ A at a cutoff voltage of $U_C = 0.5$V and at room temperature. There is a difference of about 3 orders of magnitude to the simulations. An increasing U_C causes an increasing dark current ($I_d = 1.4 \cdot 10^{-10}$ A at $U_C = 30$V). The reason is the increasing width of the space charge region d_s with increasing U_C:

$$d_s = \left(\frac{2\varepsilon_H(U_D - U_C)(N_A + N_{D)}}{eN_AN_D} \right)^{1/2} \qquad (1)$$

In eq. (1) U_D means the diffusion voltage, N_A and N_D are the concentration of acceptors and donors, respectively, ε_H is the dielectric constant and e = $1.6 \cdot 10^{-19}$ As is the elementary charge.

Dark currents measured at room temperature on diodes prepared on bonded hydrophobic wafer pairs are about 1 order of magnitude higher ($I_d = 1.1 \cdot 10^{-10}$ A) than for the wafers having an epitaxial layer of the same thickness (30 µm). The dark current, however, is decreasing if the top layer thickness increases to 50 µm ($I_d = 2.6 \cdot 10^{-11}$ A) which is nearly equivalent to the value measured for diodes on epitaxial material.

a)
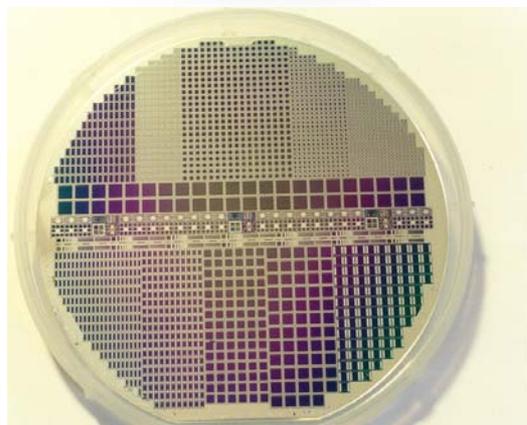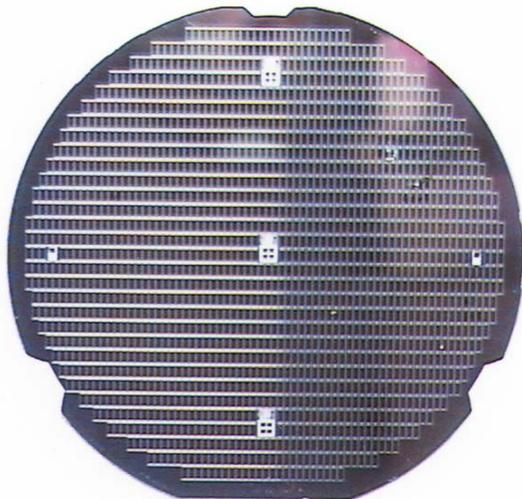
b)

Figure 1: Images of bonded wafer pairs after complete CMOS processing (wafer diameter 4in.).
  a) Bonded hydrophobic wafer pair.
  b) Bonded hydrophilic wafer pair (SOI).

Furthermore, the dark current of diodes prepared on SOI wafers is significantly higher ($I_d = 5.0 \cdot 10^{-10}$ A). Increasing the measurement temperature increases also the dark current (Fig. 2). The slope of the curve measured for diodes on the epitaxial material, however, is higher so that I_d becomes similar or higher than for diodes on bonded hydrophobic wafers even at T ≥ 140°C. This let us assume that thermally stimulated generation processes in the intrinsic layer (epitaxial layer) mainly contribute to the dark current. Carrier generation processes on the bonded interfaces appears to be less important. This interpretation is also confirmed by the fact that the differences of I_d increase at higher cutoff voltages (which causes the extension of the space charge region up to the bonded interface). For instance, a dark current of $2.1 \cdot 10^{-5}$ A results for diodes on epitaxial wafers at T = 160°C (U_C = 30V), while $I_d = 1.1 \cdot 10^{-5}$ A is measured for diodes on bonded hydrophobic wafers under the same conditions. In addition, the measurements also revealed higher dark currents of pin-diodes prepared

on SOI wafer. Differences of about 1 order of magnitude are obtained also at elevated temperatures. But the slope of the curve of I_d = f(T) is lower at higher temperatures which may refer to similar values of the dark current at T > 200°C for the SOI material. A similar behaviour of the dark current described for individual pin-diodes was also obtained for the complex MOEMS.

Besides the dark current the photocurrent was also analyzed. Photocurrents measured on pin-diodes (1 x 1 mm²) prepared on epitaxial wafers of different layer thickness. The current is between $1 \cdot 10^3$ nA and $2.5 \cdot 10^3$ nA depending on the layer thickness. Furthermore, measurements on diodes prepared on hydrophobic bonded silicon wafers show an analogous or higher photocurrent. The highest photocurrents ($5.5 \cdot 10^3$ nA ≤ I_p ≤ $7.5 \cdot 10^3$ nA) were measured for diodes prepared on SOI wafers. The photocurrent is increasing as the thickness of the top layer increases (corresponding to an increasing thickness of the intrinsic layer).

Measurements of the capacity of photodiodes as a function of the cut off voltage (CV-curves) were also carried out. The data for diodes prepared on epitaxial wafers proved the dependence of the capacity on the thickness of the epitaxial layer, i.e. the highest values of the capacity were obtained for the thinnest epitaxial layer (thickness 15 µm). This result agrees with the general assumption of the capacity of the space charge layer which is given as

$$C_s = A \frac{\varepsilon_H}{d_s}, \qquad (2)$$

where A is the active area. Using eq. (1), the capacity can also be expressed as

$$C_s = A \left(\frac{e \varepsilon_H N_A N_D}{2(N_A + N_D)(U_D - U_C)} \right)^{1/2}. \qquad (3)$$
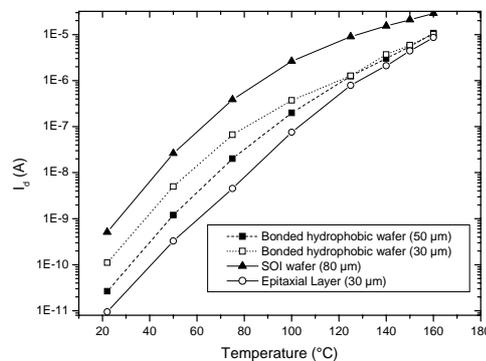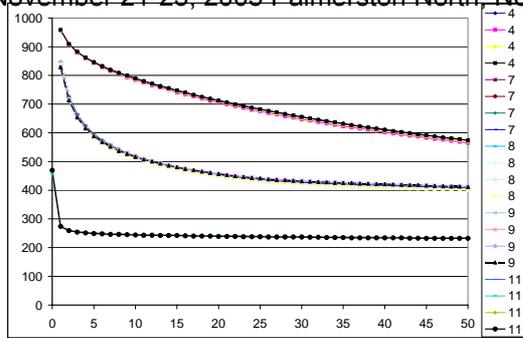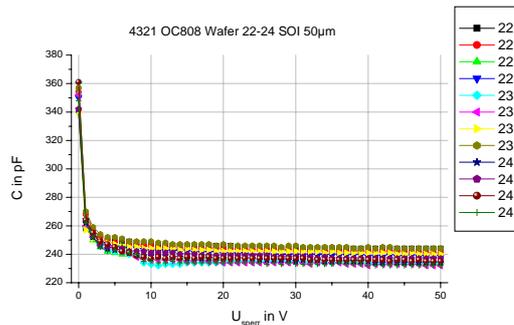
This means that the capacity of the space charge

Figure 2: Measured dark currents of pin-diodes (active area 3.7 mm²) as a function of the measurement temperature for the different materials used. The cut off voltage is 0.5 V.

a)

b)

Figure 3: CV-curves of pin-diodes prepared on epitaxial wafers (a) having layers thicknesses of 15 µm (top), 30 µm, and 50 µm (bottom).
CV-curves of pin-diodes prepared on bonded hydrophobic wafers (layer thickness 50 µm). The area of the diodes (OC 808) is 100mm² (b)

region depends mainly on their depth. C_s decreases as the depth of the space charge region increases. If the depth is limited (by the thickness of the epitaxial layer) the capacity is constant. CV-curves were also measured on diodes prepared on bonded hydrophobic wafers. An analogous behaviour of the CV-curves was found if the same thickness of the top (intrinsic) layer is assumed (Fig. 3b).

Furthermore, the rise time was measured for different pin-diodes prepared on epitaxial wafers and on bonded hydrophobic wafers. The thickness of the epitaxial layer (or the top layer for the bonded wafer) was 50 µm. Diodes on epitaxial wafers result in rise times between 21.6 ns and 23.1 ns. On the other hand, the rise time measured on diodes on bonded hydrophic wafers is between 15.6 ns and 17.1 ns. Shorter rise times (as obtained for the bonded wafers) refer to a lower diffusion current contributing to the photocurrent. This means that diodes with higher switching frequencies can be realized on the bonded hydrophobic wafers instead of the conventional epitaxial material.

4   Conclusions

The investigations proved that bonded wafer pairs can be successfully applied to the preparation of components and complex MOEMS. Especially bonded hydrophobic wafer pairs are substrates comparable to conventional epitaxial wafers. The advantages of the bonded materials are (i.) the flexibility for different material combinations which cannot be realized by epitaxy processes, (ii.) the variability of the layer thickness, and (iii.) the reduced production costs.

The preparation of different photodiodes (pin-diodes) demonstrates that important parameters of these sensitive devices are comparable or better by application of the bonded hydrophobic wafers. Especially the dark current measurements proved that the interface produced by hydrophobic wafer bonding does not act as generation source of carriers. There are no electrically active impurities on the interface. In addition, the higher values of the dark current measured on diodes prepared on SOI wafer are probably caused by such electrically active impurities in the interface. An additional cleaning process before hydrophilic bonding could improve this behaviour.

Devices prepared on bonded wafers are now applied in the fabrication of emitter-detector modules used as distance sensors and for precision instruments. Other applications are in progress.

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