1st International Conference on Sensing Technology
November 21-23, 2005 Palmerston North, New Zealand

High Dynamic Range Sensor Active Pixel Sensor

Thalis Anaxagoras[1], Nicola Guerrini[2], Renato Turchetta[2] and Nigel M. Allinson[1],

[1] Department of Electronic and Electrical Engineering, University of Sheffield, S1 3JD, UK

[2] Rutherford Appleton Laboratory, CCLRC, Chilton, OX11 0QX, UK

T.Anaxagoras@rl.ac.uk

Abstract

We are implementing a new pixel test structure in a 0.25 μm CMOS process. This new structure is based on an internal pixel circuit that resets the pixel each time the well-capacity nears saturation and an analogue memory (counter), implemented in the pixel itself, records the number of resets per integration period. The increase in the dynamic range (DR) is *(m+1)* where *m* is the number of resets per period. The peak signal-to-noise ratio (SNR) will be increased due to the effective increase in the well capacity.

Keywords: Active pixel sensor, high dynamic range, signal to noise ratio, analogue memory

1 Introduction

Active Pixel Sensors (APSs), based on conventional CMOS technology, are expanding rapidly in application and performance. They offer some significant advantages over CCDs, notably in terms of cost and ease of design [1-2]. The past few years has seen a considerable effort to increase the Dynamic Range (DR) of APSs. One of the most widespread methods is the use of a logarithmic response to the incident illumination [3-5]. Despite the logarithmic pixel structure achieving a very high DR, the non-integrating nature of the sensor limits the achievable SNR for even high illumination situations due to the exponential transconductance relationship. In addition many applications require the accurate detection of small intensity variations on a large background level (e.g. absorption spectroscopy). The proposed structure increases the effective well capacity of the pixel without compromising the SNR (Figure 1). An important advantage of this scheme, over other DR enhancement schemes, is that the digitised output is linear with illumination. Some previous research has been undertaken in this area. In [6] the authors describe a photocurrent estimation algorithm for a self-reset pixel. This estimation is based on the assumption that linear illumination is applied to the sensor which is not true for all types of applications. Another demonstration is described in [7], where the DR of sensor is enhanced by recording the time that the first internal reset occurs.

2 Proposed architecture

2.1 Concept and basic operation

Our concept is based on an in-pixel comparator used to compare the photovoltage produced during exposure with a reference voltage which sets a lower limit to the pixel voltage just prior to the well capacity becoming fully saturated. When the pixel voltage goes below this reference, the comparator triggers, the internal reset circuit resets the pixel and the counter increases its current value by one. If *m* is the maximum number of resets that can be counted in the pixel then the total available pixel full well capacity is multiplied by *m+1*.

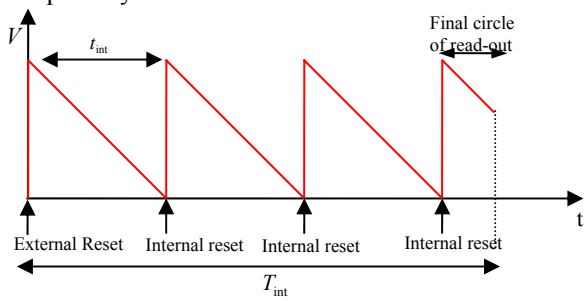

Figure 1: High dynamic sensor: pixel operation voltage output

In our test structure we consider three different pixel designs. Here we are present only one type of comparator and only an analogue memory implementation.

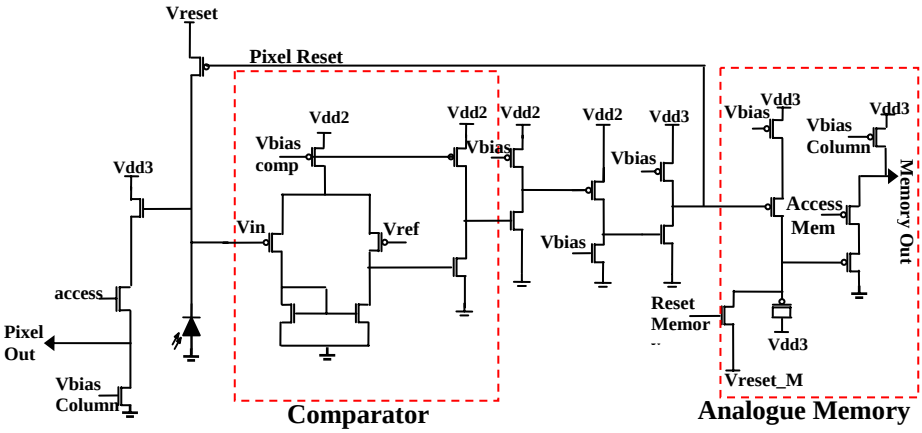

Figure 2: Pixel architecture

2.2 Design

The HDR pixel is shown in Figure 2. By initially setting the reference voltage (V_{ref}) the pixel is reset. Then the reference voltage is set to a lower voltage to allow the exposure time to begin. During exposure, the photovoltage is compared with the reference voltage, if it goes below the set reference voltage then the comparator triggers and an internal reset pulse is produced to reset the pixel. Furthermore, it is important that the comparator triggers before the well capacity is fully utilised. This is to prevent pixel saturation and so ensures response linearity.

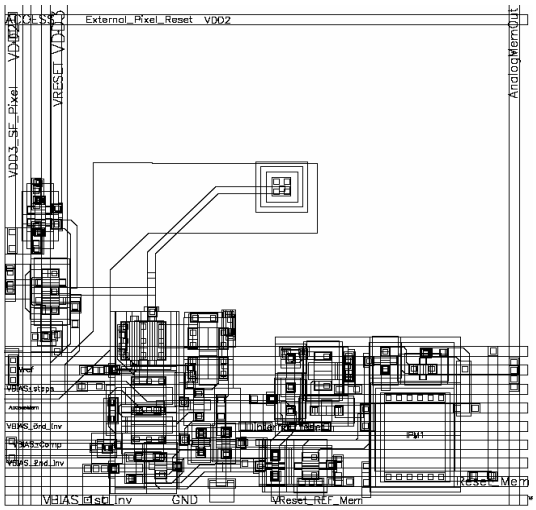

Figure 3: Pixel layout

A series of inverters ensures that the reset pulse in the feedback loop will return to 0 V for a sufficient time that the diode will reach the desired reset voltage. This can be achieved by controlling the biasing voltages of the inverters (V_{bias}) which set the reset pulse width.

At the same time, charge is injected into the pmos-capacitor (analogue memory). The step size of the memory is controlled by the biasing voltage of the analogue memory.

Since the charge is injected into a non linear capacitance, the step increments are non linear but the height of each step is sufficiently large so that they can be delineated up to the n^{th} step (see Figure 4). In our case n is of the order of 16. To achieve greater linearity, the memory is not reset to 0V but to V_{reset_M}. The advantage of this type of memory structure is its compact layout, which positively effects the available fill factor.

Simulations reveal that the charge injected into the capacitor is also dependent on the reset pulse time. The duration of this pulse depends on the slope at the input of the comparator, so that the height of each step has some dependence on the incident flux. For example, 20 ns reset pulse difference will inject more charge making our memory unable to count more than five. This is however an extreme case and should not affect the normal performance of the sensor significantly.

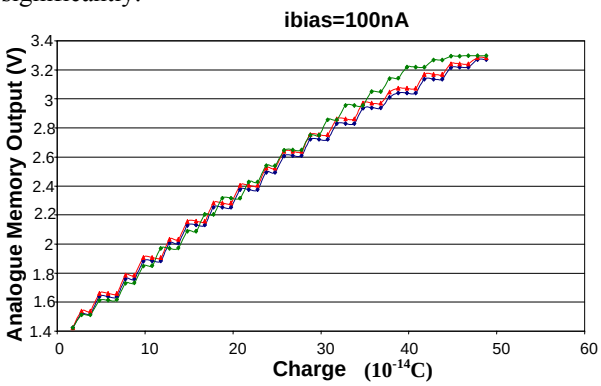

Figure 4: Analogue memory simulations (Red: 10 µs pulse at beginning of exposure, Blue: 10 µs pulse at end of exposure, Green: uniform illumination)

Further we took into account the change in the memory voltage if the same amount of charge (spike) is injected to the diode at different time during exposure time. In the worst case scenario there is a

small change in voltage which does not cause significant problem. The plot in Figure 4 illustrates our simulation observations.

During readout, the charge remaining in the photodiode is read out in the same way as in a traditional 3T APS. The reference voltage is set to ground to avoid any further reset.

Table 1: Pixel characteristics

Technology	0.25µm CMOS
Pixel size	30µ x 30µ
Conversion Gain	41µV/e^-
Fill Factor	60%
Counter maximum count	m =16
Supply Voltages	3.3V and 2.5V
Well capacity	≈$(m+1)$60000e^-
Total well capacity (m =16)	1020000e^-
Transistor per pixel	22
Reset Noise	$\approx\sqrt{(m+1)}$ 25e^-
Total Reset Noise (m =16)	≈103e^-
Internal reset noise contribution	$\approx\sqrt{(m+1)}$ 3.8e^-
Total Internal reset noise contribution (m =16)	≈ 16e^-

To reduce the power consumption in the pixel, the comparator was designed to work with a 2.5 V power supply, while the reset and the source follower operate at 3.3 V to maintain a HDR. Low power consumption is very crucial. In the case of uniform illumination, all pixels should have similar behaviour. This will cause all of them to reset at the same time, causing a large drop on the power supplies which can deactivate or slow down some of the comparators in the array. Possibility has been accounted for both the design and the layout process.

3 Noise Consideration

3.1 Reset Noise

Since a PMOS transistor is employed to reset the diode, a hard reset is produced which gives a reset noise power:

$$\overline{V_{\mathrm{Re}set}^2} = (m+1)\frac{kT}{C} \tag{1}$$

3.2 Readout Noise

The readout noise is determined by the internal reset configuration (i.e., comparator and inverters noise sources) and the signal readout scheme, which is identical to the conventional 3T APS scheme.

3.2.1 Internal reset noise contribution

Assuming that a pmos-input differential pair is used (Figure 5), the noise component of the comparator can be split into two elements the sampling phase and the slewing phase [8].

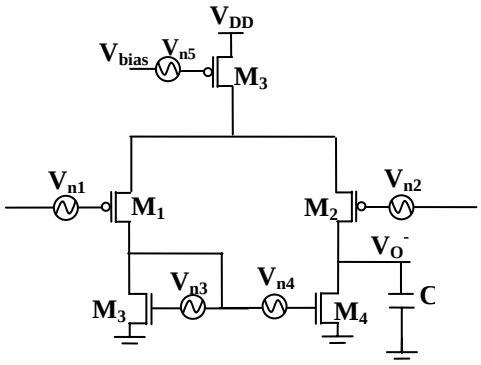

Figure 5: Differential pair noise model

To simplify the equations, noise will be analyzed at V_O^-, by assuming symmetry. Considering the reset phase first, the total sampling noise at V_O^- due to M_2 and M_4 at the end of the reset phase is approximately [8]:

$$\overline{V_{sampling}^2} = (4kTR_{on4} + \frac{8}{3}kTg_{m2}R_{on4}^2)f_{NBW} + \frac{K_{fn}I_{D4}}{L_4^2C_{ox}}\ln\left(\frac{f_{high}}{f_{low}}\right) \tag{2}$$

where R_{on4} is the 'on' resistance of M_4 and f_{NBW} is the noise bandwidth during reset, f_{high}, and f_{low} are the integration limits for the flicker noise. The noise bandwidth is given by:

$$f_{NBW} = \frac{\pi}{2}f_{-3dB} = \frac{1}{4R_{on4}C} \tag{3}$$

where C is the load capacitance at V_O^-.

The flicker noise of M_2 is not included in the reset sampling noise of Equation 2. Flicker noise can be analyzed as part of the slewing phase. The total flicker noise current in M_2 is:

$$\overline{i_{1/f,tot}^2} = \frac{K_{fp}2I_{D2}\mu_n}{L_2^2}\ln\left(\frac{f_{high}}{f_{low}}\right) \tag{4}$$

Therefore the total noise at V_O^- due to the flicker noise in M_1 as a function of time is:

$$\overline{V_{flicker}^2(t)} = \left(\sqrt{\overline{i_{1/f,tot}^2}}R_{on4} + \frac{\sqrt{\overline{i_{1/f,tot}^2}}}{C}t\right)^2 \tag{5}$$

The first term represents an initial error and the second accounts for the integrated noise. The thermal

noise component of M_1 on the other hand cannot be consider constant, as it changes slightly as a function the integration time. When integrated, the total squared charge error at the output node due to thermal noise is [8]:

$$\overline{q^2_{thermal}(t)} = \frac{1}{2}\frac{\overline{i^2_{thermal}}}{\Delta f}.t = \frac{4}{3}kTg_{m1}t \qquad (7)$$

Combining the thermal and flicker noise integrals, the total output noise voltage power as a function of time for the slewing phase is given by:

$$\overline{V^2_{slew}(t)} = \frac{\overline{q^2_{thermal}(t)}}{C^2} + \overline{V^2_{flicker}(t)} \qquad (8)$$

The total noise for the differential pair is equal to the sum of the sampling noise and the slewing noise powers:

$$\overline{V^2_{n\_comp,tot}(t)} = 2.\left(\overline{V^2_{sampling}} + \overline{V^2_{slew}(t)}\right) \qquad (9)$$

where the factor of 2 accounts for noise in both branches of the differential pair. Referring the total noise to the input, the output noise must be divided by the square of the effective differential gain of the comparator:

$$A_{eff}(t) = \frac{g_{m2}t}{C} \qquad (10)$$

With the resulting input referred noise voltage of the comparator as:

$$\overline{V^2_{in,eq}(t)} = \frac{\overline{V^2_{n\_comp,tot}(t)}}{A^2_{eff}(t)} \qquad (11)$$

The noise due to the amplification stages (Figure 6) of the feedback loop can be considered negligible since the dominant noise source will be that of the differential pair.

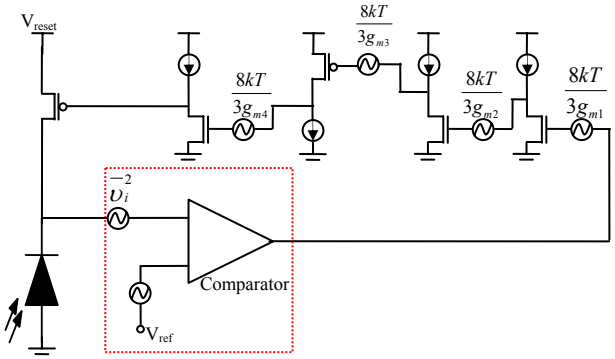

Figure 6: Noise model for the HDR pixel

For a more accurate noise calculation, the noise of the first inverter is considerd (Figure 7).

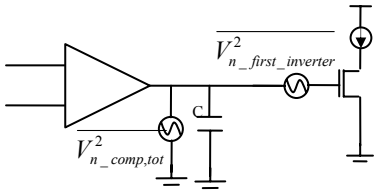

Figure 7: Noise model including the first inverter stage

The input referred noise due to the first inverter stage is given by:

$$\frac{\overline{V^2_{n\_first\_inverter}}}{\Delta f} = \frac{K_f}{WLC_{ox}f} + 4kT\frac{2}{3}\frac{1}{g_m} \qquad (12)$$

so the equivalent input noise of the differential pair can be rewritten as:

$$\overline{V^2_{in,eq}(t)} = \frac{\overline{V^2_{n\_comp,tot}(t)} + \overline{V^2_{n\_first\_inverter}}}{A^2_{eff}(t)} \qquad (13)$$

The analogue memory noise contribution in the signal will be mainly due to the enable transistor connected in the feedback loop. This again can be ignored for the overall noise estimation, since is not a dominant noise source.

Given a typical slew time of approximately 100 ns, the input referred voltage of the comparator is:

$$V_{in,eq,rms} = \sqrt{\overline{V^2_{in,eq}}(t = 100ns)} = 0.155mV \qquad (14)$$

From simulation the noise was estimated to be $0.25m$V.

3.2.2 Residual Photo-signal readout noise

The remaining signal in the well read out using the conventional the column source follower circuit (Figure 8).

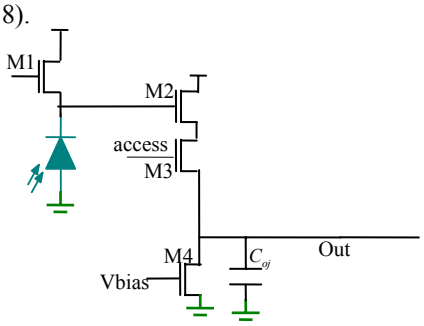

Figure 8: 3T voltage-mode pixel schematic

The noise in this case is [9]:

$$\overline{V^2_{n,read,M2}} = \frac{2}{3}\frac{kT}{C_o}\frac{1}{1+\frac{g_{m2}}{g_{d3}}} \qquad (14)$$

$$\overline{V_{n,read,M3}^2} = \frac{kT}{C_o}\frac{1}{g_{d3}\left(\frac{1}{g_{d3}}+\frac{1}{g_{m2}}\right)} \quad (15)$$

$$\overline{V_{n,read,M4}^2} = \frac{2}{3}\frac{kT}{C_o}g_{m4}\left(\frac{1}{g_{d3}}+\frac{1}{g_{m2}}\right) \quad (16)$$

3.3 Fixed Pattern Noise

Fixed-pattern noise is defined as the spatial variation in pixel output values under uniform illumination due to pixel mismatches across a sensor. Montecarlo simulations have not been performed because there are no parameters available on the statistics of the foundry process. Hand calculations have shown that the expected FPN is less than 0.7% of one full voltage swing.

If the sensor is restarted sufficient times during the overall integration period pixel noise will be effectively negligible since there will be a significant output signal and shot noise will dominate.

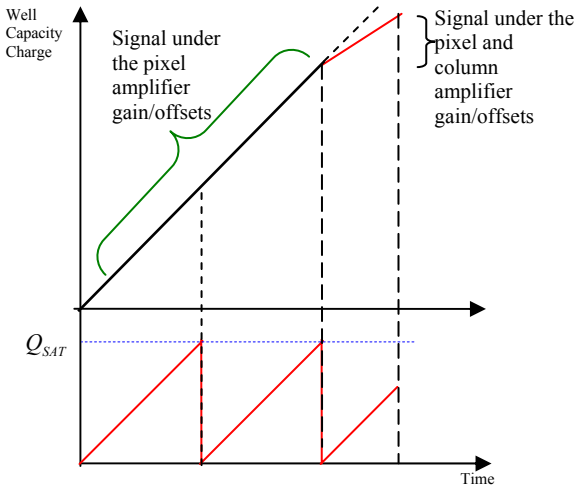

Figure 9: Well capacity vs. time.

One concern is the case where some pixels restart one or twice while others not at all; then there will be marked variations in the gains/offsets between pixels causing appreciable gain/offset FPN in the image. Figure 9 shows the gain/offset variations at different stages of operation. A one-time calibration procedure is normally used to counteract the effect of these fixed variations but in this case it is not straightforward procedure as different calibrations parameters have to be obtained for the different situations. We have developed various test structures for FPN reduction which might provide a solution if FPN is a dominant effect [10].

4 Signalto-Noise Ratio and Dynamic Ratio

4.1 Signal-to-Noise Ratio

The maximum signal to noise ratio is given by:

$$SNR_{HDR}(i_{ph}) = 10\log_{10}\frac{i_{ph}^2}{\frac{q^2}{T_{\text{int}}^2}\left(\frac{1}{q}(i_{ph}+i_{dc})T_{\text{int}}+(m+1)\sigma_r^2\right)}\,dB \quad (17)$$

where $\sigma_r^2 = \sigma_{\text{Reset}}^2 + \sigma_{\text{Readout}}^2 + \sigma_{Internal\_reset}^2 electron^2$

Figure 10 shows that the pixel architecture should not introduce any additional noise and for high photon intensity the noise is dominated by the photon shot noise.

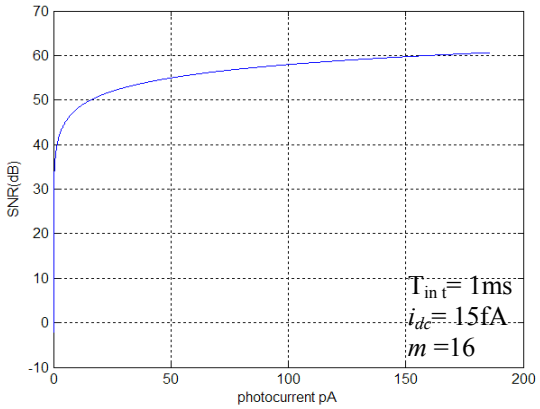

Figure 10: Signal -to-Noise Ratio vs. photocurrent

4.2 Dynamic Range

The DR is defined as the ratio of the largest nonsaturating input signal to the smallest detectable input signal. The maximum non-saturated signal in this type of sensor given by:

$$i_{\max} = \frac{(m+1)qQ_{sat}}{T_{\text{int}}} - (m+1)i_{dc} \quad (18)$$

where i_{dc} is the photodiode dark current.

The smallest detectable signal is defined as the standard deviation of the input referred noise under dark conditions and is assumed to be equal that of the traditional 3T pixel since reset noise is the dominant noise source for low illumination:

$$i_{\min} = \frac{1}{T_{\text{int}}}\sqrt{qi_{dc}T_{\text{int}}+\sigma_r^2} \quad (19)$$

The DR equals:

$$DR_{HDR} = 20\log_{10}\frac{i_{\max}}{i_{\min}} = 20\log_{10}\frac{\frac{q(m+1)Q_{sat}}{T_{\text{int}}} - (m+1)i_{dc}}{\frac{q}{T_{\text{int}}}\sqrt{\frac{1}{q}i_{dc}T_{\text{int}} + \sigma_r^2}} \quad (20)$$

$$DR_{HDR} = 20\log_{10}(m+1) + 20\log_{10}\frac{\frac{qQ_{sat}}{T_{\text{int}}} - i_{dc}}{\frac{q}{T_{\text{int}}}\sqrt{\frac{1}{q}i_{dc}T_{\text{int}} + \sigma_r^2}}$$

The increase in DR is of the order $20\log_{10}(m+1)$. In simulations we achieve a maximum m of 16, which corresponds to an increase of 24.6 dB in the DR with respect to a traditional APS.

5 Conclusion

The underlying concept of a HDR pixel structure has been presented and simulation results show enhanced DR and SNR due to the multiple utilisation of the well capacity of the pixel's photodiode. A test structure is being designed in a 0.25 μm CMOS process and tests results will be presented when available. The DR can be extended further by multiple read out of analogue memory during the overall exposure time.

6 Acknowledgements

This work is part of the UK Basic Technology Programme, Multi-dimensional Intelligent Integrated Imaging Project (EPSRC Ref. GR/S85733/01).

7 References

[1] E. R. Fossum, "Active pixel sensors: are CCD's dinosaurs?," *Proceedings of the SPIE - The International Society for Optical Engineering, Charged-Coupled Devices and Solid State Optical Sensors III, 2-3 Feb. 1993*, vol. 1900, pp. 2-14, 1993.

[2] E. R. Fossum, "CMOS image sensors: electronic camera-on-a-chip," *IEEE Transactions on Electron Devices*, vol. 44, pp. 1689-98, 1997.

[3] E. C. Fox, J. Hynecek, and D. R. Dykaar, "Wide-dynamic-range pixel with combined linear and logarithmic response and increased signal swing," *Proceedings of the SPIE - The International Society for Optical Engineering Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications, 24-26 Jan. 2000*, vol. 3965, pp. 4-10, 2000.

[4] M. Loose, K. Meier, and J. Schemmel, "A self-calibrating single-chip CMOS camera with logarithmic response," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 586-596, 2001.

[5] Y. Oike, M. Ikeda, and K. Asada, "High-sensitivity and wide-dynamic-range position sensor using logarithmic-response and correlation circuit," *IEICE Transactions on Electronics*, vol. E85-C, pp. 1651-1658, 2002.

[6] X. Liu and A. El Gamal, "Photocurrent estimation for a self-reset CMOS image sensor," *Proceedings of the SPIE - The International Society for Optical Engineering, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications III, 21-23 Jan. 2002*, vol. 4669, pp. 304-12, 2002.

[7] J. Rhee and Y. Joo, "Wide dynamic range CMOS image sensor with pixel level ADC," IEE *Electronics Letters*, vol. 39, pp. 360-361, 2003.

[8] Michael D. Scott, "An Ultra-Low Power ADC for Distributed Sensor Networks", Research Project, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley.

[9] H. Tian, B. Fowler, and A. El Gamal, Analysis of Temporal Noise in CMOS APS, In *Proceedings of the SPIE Electronic Imaging '99 conference*, Volume 3649, January 1999.

[10] Thalis Anaxagoras, Renato Turchetta, Nigel Allinson, Simon Triger, "APS Column Fixed Pattern Noise Reduction", Workshop on Charge-Coupled Devices and Advanced Image Sensors, IEEE, pp.76-79, 9-11 June 2005.