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Behavioral Model for System Level Design Automation: Passive UHF Transponder Case Study

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Abstract

Sensor telemetry applications and contact-less identification utilize the advantage of long range, remotely powered transponders. The RF power signal at 900 MHz carrier frequency is an energy and data carrier. In reality the operability of remote passive RF tags is decreased by field distortions due to surrounding objects, environmental noise, and collision with other wireless devices. To support first-time-right design the IC development and system integration are supported by simulations. The prime focus here is on the radio frequency link, the tag front-end and the verification of the implementation of the digital logic. A behavioral model of analog and digital parts of an RFID tag is presented. Hardware-in-the-loop simulation is then described to verify the model of digital parts in a real environment.

Keywords: transponder, RFID, UHF, sensor tag, DSP

1 Related Work

Radio frequency identification (RFID) enables fast tracking and identification of objects labeled with RFID tags. Passive UHF (Ultra High Frequency) transponders collect the power from modulated incident RF signal, which is also the data carrier. Passive tags transmit data back to the interrogator by backscattering (figure 1).

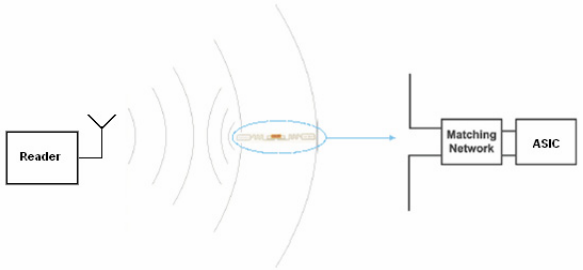

Figure 1: Principle of passive UHF transponders

The next generation of RFID transponders extends the tags' original identification purpose by embedding sensors. In particular, the UHF band (860-960 MHz) offers specific advantages such as high data rates and a long reading range. Unlike RFID systems in the lower frequency bands, the standards defining UHF systems are quite new. Developed products should comply with these standards. To save time and costs during the development process, the prototype implementation phase should be minimized. This necessitates developing an accurate and practical means of testing the hardware and software modules.

An appropriate method for this is the Hardware-In-the-Loop (HIL) simulation. A testing module - implemented in hardware - is connected to the real-time running model using special hardware and software interfaces. Using this module, it is possible to test the system in real-time. This testing method has been tried and proven in other sectors such as the automotive industry (e.g. controllers for engine and gearboxes).

This paper describes a behavioral model of UHF transponders and a HIL simulation module for model-based verification of UHF RFID system design (see figure 2). This module simulates one part of the system while being connected to the other real components. The potential applications of such a HIL module include environment modeling, testing of various communication protocols and implementations of readers and tags, as well as the simulation of a wide range of real world scenarios.

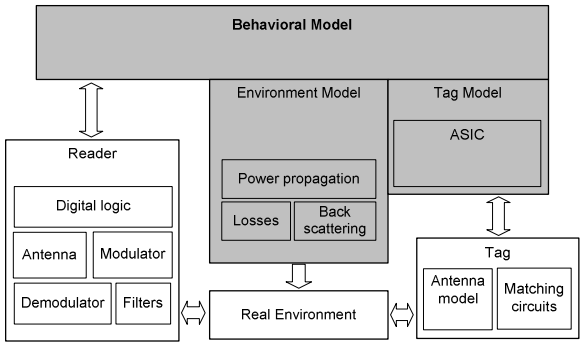

Figure 2: HIL verification of tag ASIC digital module design

High tag reading rates can be achieved using a high bandwidth for the communication. Current communication rates range from 40 kbps to 640 kbps. The next critical factor is the DC current consumption, which has a direct impact on the communication range. This is an important research topic in the field of RFID. Currently, tags consume 5-

10µW DC during reading and 10-20µW DC during writing. The efficiency of the power conversion η is about 20 %, which implies that a tag requires 20-50µW in the read mode and 50-100µW in the write mode. By assuming the minimum power for reading tags to be 50µW, this corresponds to -43db [1]. Recent development [2] achieved less than 20µW minimum RF input power for a PSK (phase shift keying) transponder.

Figure 3 is based on empirical studies and displays the relationship between the required EIRP of the reader and the distance to the tag.

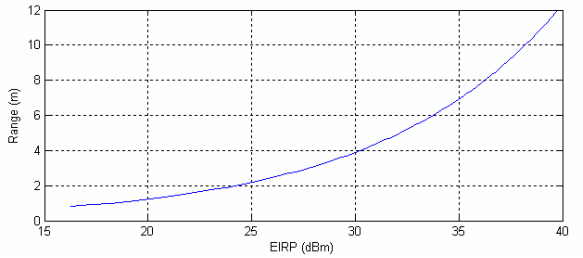

Figure 3: Achieved communication distance based on RF power transmitted by a reader

2 System Level Design Automation for RFID devices

In developing of software, individual software modules were tested both separately as well as in the context of the entire complex system. Hardware-in-the-Loop simulation method enabled for testing heterogeneous systems. Because of the simulated virtual (and reproducible) environment and the restorable (saved) set of test patterns, HIL simulation is completely reproducible. Thus, it is possible to make direct comparisons between simulations with different parameter settings. Optimizing the system performance is done in a model with less effort than on a prototype. Real-time interaction and a feedback from other RFID devices in a specific environment are essential.

3 Case study: Model based design of an UHF transponder

The tag model has been build out of three components: antenna, matching circuitry and ASIC (Application Specific Integrated Circuit).

3.1 RF front-end and analog modules

Since the dynamic response of the radio frequency part (RF front-end) of the tag is 10^3 times faster than the low frequency circuitry in the ASIC, the high frequency parts have been modeled as a RLC circuit as depicted in figure 4.

L_a and R_a stand for tag antenna inductance and resistance, respectively. C_p represents the ASIC parasitic capacitance and R_p the ASIC parallel resistance. U_0 is the voltage that could be observed on the antenna with no load connected to it.

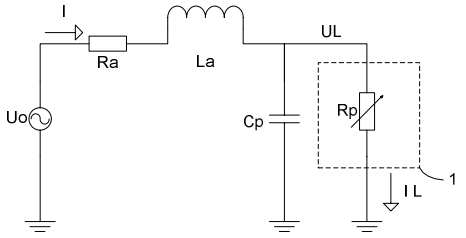

Figure 4: RLC circuit model of an RF-transponder

Tag ASIC is built of the modulator, demodulator, voltage controllers, rectifier, voltage multiplier, and digital logic. Modern tags embed also sensors on the chip. This structure allows modeling any potential architecture of the ASIC based on the description of the current through individual blocks as a function of the input voltage (see figure 5).

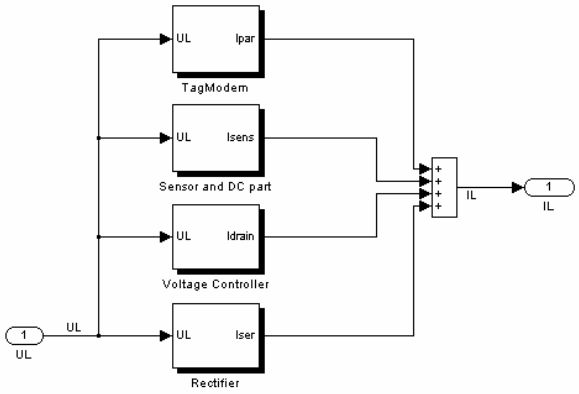

Figure 5: Block model of tag ASIC with a sensor module

The data flow from the tag to the reader is realized using backscattering. The tag modulator in the ASIC changes the modulating current, therefore changing the ASIC impedance, which in turn causes mismatch between the ASIC and the antenna. Less power is collected by the tag and more power is reflected back to the reader during backscattering.

Critical for the tag functionality is the DC voltage (VDD) level. The minimum VDD required for the functionality of the RFID transponder is above 1V for the newest designs. As shown in figure 6 VDD is proportional to the voltage U_L that appears across the signal pads of the ASIC.

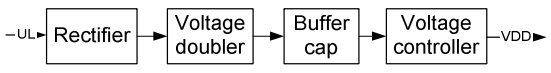

Figure 6: DC voltage generation

Figure 7 shows the dependency of the optimum ASIC load current I_L on the RF input power magnitude P_{tag} to reach the maximum supply voltage.

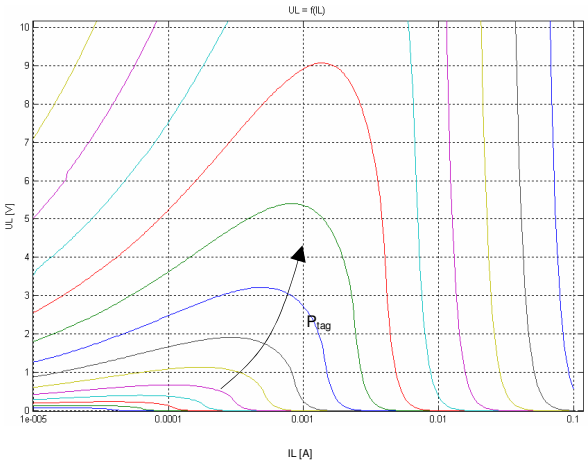

Figure 7: ASIC load voltage magnitude U_L as a function of load current magnitude I_L and RF input power magnitude P_{tag}

3.2 Model evaluation using HIL Simulation

Model-based evaluation of potential architectures of the tag ASIC is one step in the proposed system level design. The target of the simulation is also to verify the compliance of the implementation of the digital part with the protocol. To verify the digital model in a real environment, a HIL simulation of an UHF RFID tag (ISO18000 - 6B compliant) has been implemented. The internal processing of the tag is emulated while the RF unit is made in hardware and is used for communicating with a real UHF RFID reader. Model of the digital logic implemented as a state-machine in Matlab/Simulink has been automatically converted into a C-code and compiled for the target architecture.

Figure 8 shows the concept of HIL simulation architecture for a tag, in which the digital unit in the tag is simulated by a real-time model implemented on a DSP board. This model sends data to the reader using a small tag emulator, which consists of the matching network (MN), an energy store unit (capacitor) and the modulating transistor.

Requirements on the target system hosting the simulation are mainly defined by the minimum sampling time of the system model. Three different time constraints have to be fulfilled:

1. Data transmitted by the reader has to be sampled by the AD converter quickly enough to ensure that no signal transitions are missed.
2. Sampled pattern must be quickly compared with the predefined pattern of the reader command and the response packet must be quickly generated to ensure that none of the commands sent by the reader are missed.
3. Computed data must be transferred to the DA converter quickly and stably enough to ensure that the output data rate is fixed at the given data rate (40 kbps).

The shortest of these time constraints determines the required step size for the model. The sampling frequency is then

$$f_{sampling} \geq 2 \cdot f_{max} \cdot \qquad (1)$$

For $f_{max} = 2 \cdot f_{data} = 80$ kbps is the sampling frequency $f_{sampling} = 160$ kHz.

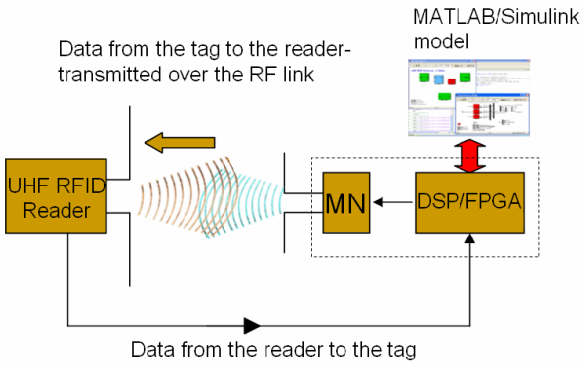

Figure 8: Concept of a HIL simulation architecture of an UHF RFID passive tag

The tag response time must not be shorter than 400 µs (a fixed quite-time) and should not exceed 1 ms according to ISO18000-6B [3]. Therefore the time window for the generation of the answer equals to the maximum of 600 µs. The generation of the tag response is the most complex task for the DSP. With the implementation on the DSP/FPGA module SMT365 from Sundance Multiprocessor Technology [4] the time for the tag response generation was 300 µs. Computation speed achieved using automatically generated code was therefore sufficient. If required the efficiency of the implementation can be further improved by modifying the generated code manually. Table 1 summarizes the minimum hardware requirements for the implementation.

Table 1: Minimum HW requirements

Interface	HW unit	Required
Analog/Digital	DSP	> 200 MHz CPU clock
Analog	A/D	≥ 160 kHz sampling
Analog	D/A	≥ 80 kHz sampling
Digital	Digital I/O serial	≥ 100 kBaud

3.3 Experimental results

The following figures show the communication between the tag emulator and real reader. The upper line shows the commands sent by the reader and the lower line indicates the response that modulates the backscattered waves.

Figure 9 shows the communication process. The tag responds to two commands transmitted by the reader. Obvious is the delay between a reader command and

the tag response, which is due to the time required to process and generate the response as well as the fixed quiet time.

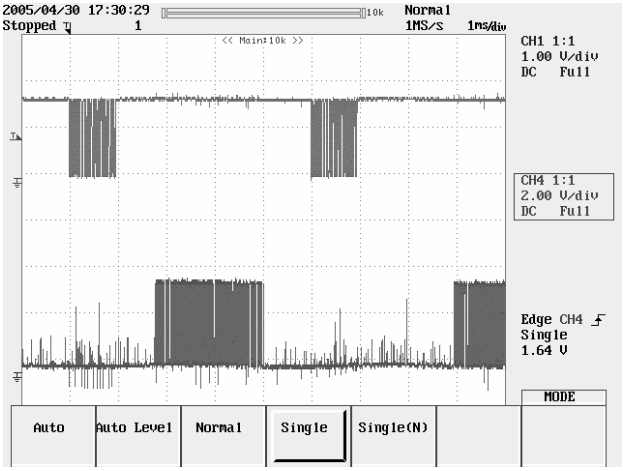

Figure 9: Commands send by the reader (upper signal) and the response from the tag emulator (lower signal)

Figure 10 displays a sequence of commands sent by the reader and followed by the tag response - one command was missed by the tag emulator - the reason was that the reader command overlapped with the response of the tag. As the tag signal is very noisy the reader evaluated the end of the tag response incorrectly and started transmitting too soon. Since the communication is half-duplex the tag emulator was then unable to detect the reader command properly.

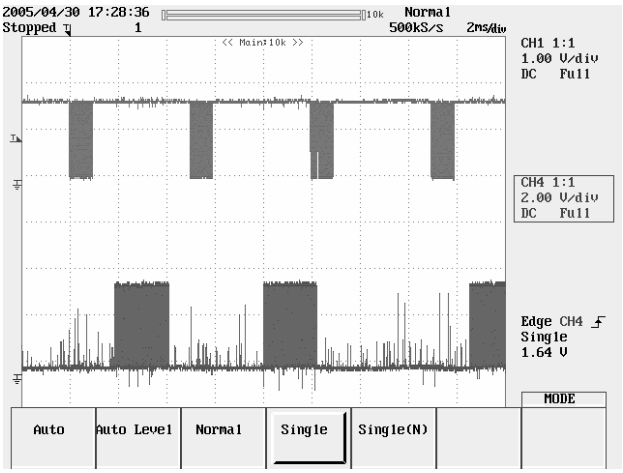

Figure 10: One reader command was missed due to the overlap or reader and tag data

The tag identification rate achieved in the simulation was 2.1 tags per second. This rate is significantly lower (by factor of 10 comparing to measurements with real products) due to the high-noise tag signal. Also the communication range of the tag emulator is 10 times lower than the range of commercial tags. Both problems are caused by not optimally matched RF structure of the emulator to the tag antenna.

4 Conclusion

Using proposed model-based design automation, it is possible to simulate various designs of analog and digital parts on the system level and to compare results with real-time simulation with hardware in the loop. Digital circuitry implementation has been simulated on the tag emulator. Limited set of commands of a communication protocol has been implemented using Stateflow in Matlab/Simulink and has been tested on a model of an UHF RFID system. Performance of the model of the tag analog parts corresponds to the specification of typical commercial products [5] and has been verified by a set of measurements. Implementation of the tag digital logic was tested in the developed model as well as on a real-time emulator of the UHF transponder. Presented HIL structure was implemented on a DSP board. A heterogeneous system with DSP and FPGA could improve the efficiency of the implementation and improved RF structure of the tag emulator can increase the communication range. Further work is ongoing in the direction of automated code generation for target platform based on C++ implementation of the full communication protocol to support the development in high programming languages.

5 Acknowledgements

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6 References

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