MASSEY UNIVERSITY
PALMERSTON NORTH CAMPUS

EXAMINATION FOR
159.253 COMPUTER SYSTEMS

Semester I - 2002

Time allowed: THREE (3) hours

THIS IS A CLOSED BOOK EXAMINATION

ANSWER ALL QUESTIONS

SECTION A
Answer ALL questions in the multi-choice section (Section A) on the Mark Sense Card provided.

28 Multi-choice Questions – each worth 1 mark 28 marks

SECTION B
Answer ALL questions in the long answer section (Section B) in the blue answer booklet provided

Three Questions – each worth 24 marks 72 marks

Total: 100 marks

Marks for each question are shown in brackets after the question, like this: [8 marks]

Note that in some of the questions in this exam, the abbreviations hi and lo have been used to signify logic high (5V for TTL, 12V for CMOS) and logic low (0V for TTL and CMOS) signals respectively.
SECTION A  
(Multi-choice Questions)

1. Each of the equations below summarises the characteristics of a particular type of digital circuit. Which set of characteristics is necessary and sufficient for sequential circuits?
   (a) output = f ( inputs )
   (b) output = f ( inputs, previous output )
   (c) output = f ( data inputs, previous history, control inputs )
   (d) output = f ( previous controller state, architecture status, inputs )  [1 mark]

2. Which of the circuits below could be used as a 6-input AND gate?
   (a) 
   (b) 
   (c) 
   (d) All of the above  [1 mark]

3. In the Truth Table below, inputs I₁ and I₀ are the bits of a two-bit number. If the Truth Table were implemented as a digital circuit, what would the circuit be called?

<table>
<thead>
<tr>
<th>I₁</th>
<th>I₀</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

   (a) A decoder  
   (b) A two-bit counter  
   (c) A full adder  
   (d) A demultiplexor  [1 mark]
4. In the above diagram of a multiplexor, the connector labelled \( \text{OE} \) …

(a) makes the output low when it is high, and high when it is low, but is superseded by the control input (2-bit address) input, when values are placed on the control input wires. Then the circuit outputs \( I_n \) when the 2-bit address is \( n \).
(b) allows the selected data input to reach the output wire when its voltage is low
(c) is an output that becomes true when output has been enabled.
(d) disables the control input (2-bit address) so that \( I_0 \) is the only data input to reach the output.

[1 mark]

5. The circuit diagram for an RS flipflop, and the voltage transition table for a NOR gate are shown at right. If \( Q \) is initially hi, what will happen to \( Q \) if \( R \) and \( S \) are set to hi and lo respectively?

(a) \( Q \) will become lo.
(b) \( Q \) will toggle repeatedly, till \( R \) and \( S \) are both set lo.
(c) \( Q \) will become lo momentarily, and then return to its original voltage.
(d) \( Q \) will remain unchanged.

[1 mark]

6. When choosing a storage device to store a bit of data temporarily, a designer would be wise to opt for …

(a) a clocked, falling-edge-triggered JK flipflop.
(b) a clocked, edge-triggered D flipflop.
(c) a clocked, rising-edge-triggered JK flip-flop.
(d) a clocked RS flipflop.

[1 mark]
7. When an address is presented to a RAM, it is “preprocessed” to generate a signal that activates a particular word in the memory. The “preprocessing” is performed by …

(a) a multiplexor.
(b) an OR gate.
(c) a tri-state buffer.
(d) a decoder.

[1 mark]

8. Shift registers can be used for …

(a) serial to parallel data conversion.
(b) simple arithmetic.
(c) parallel to serial data conversion.
(d) all of the above.

[1 mark]

9. Shift registers

(a) are used to move information from one register to another when a processor is performing a register shift operation such as \textit{mov A, r0}
(b) are the major component of RAM.
(c) do not usually require address decoding circuitry.
(d) store the status of control keys (the \textit{alt} key, the \textit{ctrl} key and, of course, the \textit{shift} key that gave them their name) to facilitate keyboard input to computers.

[1 mark]

10. In a binary up-counter, a high order bit will have the inverse of its previous value (i.e., it will have toggled) when …

(a) all the higher order bits of the \textit{new} number are 1s.
(b) all the higher order bits of the \textit{new} number are 0s
(c) all the lower order bits of the \textit{new} number are 0s
(d) all the lower order bits of the \textit{new} number are 1s

[1 mark]

11. Synchronous counters …

(a) are organised so that their flipflops are clocked at different times.
(b) have a clock input that ensures all the flipflops that are going to toggle, toggle simultaneously.
(c) do not have to have a clock input.
(d) must be clocked at regular intervals.

[1 mark]
12. In a typical ASM (Algorithmic State Machine) …

(a) there is a single sequence of states that repeats indefinitely, without any outside influence except initiation and termination.
(b) the number of states should never be a power of two, because you need to reserve the number 0 for a wait phase before the ASM enters the real states.
(c) there are generally alternative sequences of states, and the path that is taken through the sequences is conditional upon one or more external signals.
(d) the number of states is a power of two, because that makes most efficient use of the flipflops in the state register.

1 mark

13. In the design of a computer processor …

(a) circuits with feedback must never be used.
(b) it is conventional to separate the components that perform data processing and the components that control the data processing components into an architecture and a controller.
(c) it is preferable to organise the data processing architecture so that it controls its own functions, rather than using a separate controller that sends control signals to the data processing architecture.
(d) the instruction set cannot be changed without changing the data processing architecture also.

1 mark

14. In designing a computer processor based on a conventional von Neumann architecture, it is essential to include the following elements:

(a) a mechanism for transferring data between pairs of storage devices, and between storage devices and calculation devices, and a mechanism for stacking data values, and addresses.
(b) level 2 cache, power-management functions, and a hard drive.
(c) a mechanism for keeping track of the current instruction, and a mechanism for deciding which of two (or more) subsequent instructions should be executed.
(d) None of the above - all of the lists contain superfluous items.

1 mark

15. The stack in the 8051 processor is:

(a) disabled during interrupt routines.
(b) located in code memory.
(c) used to provide indexed offset addressing for subroutine parameters.
(d) used for subroutine calls and interrupt processing.

1 mark
16. The braces in the programming language C (eg. if (M>N) { ... } ) are used to group statements. An equivalent assembler construct:

(a) is always implemented with conditional jumps (eg JZ, JNZ ...).
(b) is needed but only when using the simulator. The real processor doesn’t need them.
(c) isn’t needed.
(d) is the ORG – END construct.

[1 mark]

17. In many processors, local variables and parameters are usually stored on the stack. This is not normally done with the 8051 processor. The reason is:

(a) The memory space available to the stack is very small and often needed for other purposes.
(b) The stack is located in code memory and can only be used for static (unchanging) data.
(c) Local variables cannot be implemented in assembler, only in high level languages.
(d) The stack is only needed for interrupts or when switching register banks.

[1 mark]

18. Register indirect instructions are important as they:

(a) enable one instruction to access different memory locations at different times.
(b) enable the overflow and carry bits to be used to detect arithmetic overflow.
(c) inform the assembler that the following code is a program.
(d) enable interrupts to be used.

[1 mark]

19. The carry bit is used to enable:

(a) the overflow in multi-byte arithmetic to be used in following operations.
(b) the 8051 to convert float variables to ints.
(c) serial communication to carry data out of the processor to memory.
(d) Boolean operations to be performed on any register in the register banks.

[1 mark]
20. If the routine OUTCH is available and displays the ASCII character corresponding to the value contained in the accumulator, what is displayed by the OUTCH call in this code?

```
mov r4,#2
mov r1,#'E'
loop: dec r1
       dec r1
       djnz r4,loop
mov a,r1
lcall putch
```

(a) r1  
(b) A  
(c) G  
(d) none of the above  

[1 mark]

21. Both polling and interrupts can be used for controlling I/O devices. Which of the following statements is correct?

(a) Although simpler, polling systems always have much slower response times than interrupt-driven systems.  
(b) Polling is more suitable than interrupts when a large number of devices need to be controlled. The simplicity of the software makes a rapid response time easy to achieve.  
(c) The hardware status bits used by the software to control I/O devices with polling are sometimes necessary with interrupt-driven systems.  
(d) The device vector for a polled device needs to be initialised before it can be used.  

[1 mark]

22. When a communications device is sending an asynchronous stream of bytes, it often inserts a start bit and a stop bit around each byte so that the receiver can successfully detect byte boundaries. If this synchronisation is lost, the receiver gets back into synch again …

(a) by “dead reckoning” - extrapolating from the speed at which the bits were arriving, and the time of the last correct byte, to get the expected start time of successive bytes, and synchronising on that information until valid synch information starts arriving again.  
(b) by locking on to the data stream only after a succession of at least five 10-bit sequences that contain the desired start-bit and stop-bit pattern have arrived.  
(c) by accepting any 8-bit sequence that is surrounded by the correct stop and start bits, even though the data sequence may itself contain bits pattern that match these.  
(d) by sending a synchronisation request to the sender, which pauses for $\frac{1}{5}$s, sends a sequence of alternating 1s and 0s, and then continues with the data stream.  

[1 mark]
23. Phase modulation …

(a) is used for encoding digital data on an analogue link, and involves encoding data as changes in the voltage of the digital signal.
(b) is used for encoding analogue data on a digital link, and involves encoding data as changes in the voltage of the digital signal.
(c) is used for encoding analogue data on an analogue link.
(d) is used for encoding digital data on an analogue link, and involves encoding bits (or bit sequences) as standardised shifts in the phase of an analogue carrier wave.

[1 mark]

24. Run length encoding …

(a) is unsuitable for transmitting text, because text does not often contain long sequences of the same character.
(b) is unsuitable for transmission of real-time data (such as video), because the processing delays involved in searching for long “runs” of data interferes with the real-time characteristics of the data.
(c) is unsuitable for transmitting image information because many images include large areas of a single colour, which are encoded inefficiently by the technique.
(d) is unsuitable for transmitting binary machine code, because it is a lossy compression technique, and machine code must be complete or it won’t run.

[1 mark]

25. Error detection is more important than error correction …

(a) when fibre optic cable is used, because error rates are negligible.
(b) when the network is highly congested, making retransmission of data expensive.
(c) when delays between transmission and receipt of data are very large.
(d) when retransmission of the data can be accomplished quickly, at low cost.

[1 mark]

26. In Hamming codes, errors are corrected …

(a) in batches of 3, 6, or 9 (or higher multiples of 3, though this happens only rarely).
(b) by a mechanism that involves determining the “address” of the corrupted bit(s) in the data, and inverting it (or them).
(c) by a mathematical process that is too complicated for humans to understand.
(d) by averaging the values of successive error codes. This is called measuring their Hamming distance.

[1 mark]
27. Statistical multiplexing …

(a) is generally a less efficient way of using a data comms link than time division multiplexing, because it does not allow the senders to schedule regular transmissions.
(b) requires that information travelling along the shared link carries an ID, so that it can be delivered to the correct destination.
(c) implements error correction by a mechanism that involves calculating the mean and standard deviation of the bits.
(d) should be used for long-distance communication because the “smeared-out” bits are less susceptible to corruption by interference from large-scale phenomena such as lightning strikes and radiation from the national grid (New Zealand is just about the right length to act as an antenna for 50Hz radiation).

[1 mark]

28. The Internet protocol…

(a) uses 256byte packets of data.
(b) runs at 56kbps.
(c) relies on ARQ error correction techniques.
(d) provides reliable end-to-end communications.

[1 mark]
SECTION B
(Long answers)

Answer questions 29 to 31 in the Blue Answer Booklet provided.

Write the numbers of the questions you have answered from this Section on the front cover of your blue answer booklet

DO NOT tie the Mark Sense Card into your Blue Answer Booklet.

29. (a) Design a circuit that inputs a serial data stream and outputs any 2-bit sequence that is preceded by a one, and followed by a zero.

(b) Design a circuit that inputs a serial data stream and outputs any 2-bit sequence that is preceded by a one, and followed by a zero, and does not overlap the previously output 2-bit sequence. Hint: use an ASM.

(c) Write a brief definition of a decoder, and show how decoders are used for addressing in RAM circuits.

(d) Draw a diagram of the data processing part of the Pico-computer, and explain how an instruction to load the accumulator with a word from memory could be implemented on this architecture.

30. (a) Write a compare subroutine that takes two eight bit parameters and compares them. The result is to be returned in the accumulator. If the parameters were referred to as X and Y, the result of the routine is

\[
\begin{align*}
-1 & \quad \text{if } X < Y \\
0 & \quad \text{if } X = Y \\
+1 & \quad \text{if } X > Y
\end{align*}
\]

Show how your routine would be used to compare the values 27 and 17.

(b) Write a version of the compare routine described in the first part of this question to compare two sixteen bit unsigned numbers. Show how your routine can be used to compare values.
Q.30(c) contd ...

(c) Write a routine called `printdec` in 8051 assembler. The routine displays the decimal value of the unsigned binary number in the accumulator when `printdec` is called. Leading zeroes need not be suppressed.

The routine `PUTCH` already exists and will print one character. Put the character to be printed into the accumulator before calling `PUTCH`.

[8 marks]

(d) A microcontroller is being configured to act as a combination lock

![Diagram of keypad and encoder]

The keypad has an output line `KeyPressed` that is high when any key (numeric or `CLEAR`) is being pressed and low otherwise. The numeric keys are processed by a 10-4 priority encoder, so that the numeric value of the highest numeric key that is being pressed is present on the four output lines of the encoder. The `Clear Key` line is only high when the `CLEAR` key on the keypad is being pressed.

The keys behave as ideal switches. That is, the logic level they produce changes to the new values when they are pressed, and only returns to the original value when the user releases the key.

Write a subroutine called `GetKey` that returns only when a key has been pressed and then released. The value returned should be 0-9 for the numeric keys and 255 for the `CLEAR` key.

[4 marks]

(e) Using `GetKey`, write the control program for the lock so that when the keys 441862 are pressed in sequence, the `Open Door` output becomes high. Pressing a key other than the next expected digit will cause the `Sound Alarm` output to become high. An exception to this is the `CLEAR` key which resets the lock so that the next expected digit is the first in the sequence.

[4 marks]
31. (a) Specify the frequencies that would be used for transmitting digital data over phone lines using FSK (frequency shift keying). Be sure you specify which frequencies are used by the device that originated the call and which frequencies are used by the device that answered the call. Draw a wave diagram showing how the bit string 010 would be represented. The diagram should represent the encoding CLEARLY.

[6 marks]

(b) Explain how the error detection technique known as parity checking works, and show what binary data would be transmitted if the following character sequence were transmitted without errors, using the block parity technique with even parity. ABCDEFG

Note: You may assume that 7-bit ASCII encoding is used. A is encoded as 65₁₀, and the succeeding characters are in ascending numeric order.

Your answer should be in the form of a rectangular array of bits, not a linear sequence.

[6 marks]

(c) (i) Define the terms FEC and ARQ and specify whether Hamming code is an FEC technique or an ARQ technique

[2 marks]

(ii) One bit of the following bitstream, (which was encoded using even parity Hamming coding and corrupted during transmission) is in error. The right-most bit is numbered 1, and the left most bit is numbered 15. The spaces are not significant

0001 1001 0010 100

Specify which bit has been corrupted. Show your working.

[4 marks]

(d) Describe how a communications system using statistical multiplexing uses virtual circuits to ensure that data is delivered to the correct destination. Consider a segment of a large network in which two sources, A and B are both about to start transferring information to a destination node D. Virtual circuits are set up in the following order:

A₁-D
B-D
A₂-D

[6 marks]