TIME ALLOWED: THREE (3) HOURS

Answer ALL questions in Section A (multi-choice) on the Scantron Card provided.
Answer ALL questions in Section B (long answers) in the blue answer booklet provided.

Marks for each question are shown in brackets after the question, thus [8]

THIS IS A CLOSED BOOK EXAMINATION

SECTION A
28 Multichoice Questions – each worth 1 mark 28 marks

SECTION B
Three Questions – each worth 24 marks 72 marks

Total: 100 marks
Section A (Multiochoice)

Answer questions 1 to 28 on the Scantron Card provided

Write your name and ID number on the Scantron Card

Do NOT write the numbers of the questions you have answered from this Section on the front cover of your blue answer booklet

Do NOT tie the Scantron Card into your blue answer booklet

1. A situation involves one Boolean input, B, and another input, C, which may have any of four states. Assuming that circuitry to encode C into a numeric value using digital logic signals exists, how many rows will there be in a truth table that lists all possible combinations of these inputs?

   (A) 2
   (B) 3
   (C) 8
   (D) 16

2. Does every term in a Boolean equation derived directly from a truth table (i.e., in un-minimised, OR-of-ANDs-form) include all the inputs?

   (A) No – only the inputs that are true need to be included.
   (B) It depends on whether you’re using positive or negative logic. Yes for positive logic, and no for negative logic.
   (C) Yes - you risk including invalid input combinations if you don’t specify all the input values.
   (D) None of the above, because this question can’t be answered definitively. It’s non-deterministic.

3. A multiplexor can be used…

   (A) to select one of a number of signals and put it onto single signal wire.
   (B) to output a signal on a single wire onto a selected one of several output wires.
   (C) to distinguish between the values of different binary encoded numbers.
   (D) to store state numbers in ASMs.

4. A full adder…

   (A) is a clock-triggered circuit that only operates when the carry-in input goes low.
   (B) can be made into a subtraction circuit by connecting its carry-in input to a subtract-enable line.
   (C) is a combinatorial circuit that calculates continuously.
   (D) is the central component in store-and-forward LANs.
5 The JK flip-flop…
(A) should only be used when toggling is required.
(B) should only be used when triggering is required.
(C) will only work on falling-edge data.
(D) has a forbidden input combination if J and K are both high.

6 A binary counter…
(A) can be used to count up and down simultaneously simply by connecting the Q outputs for up-counting and the ~Q outputs for down-counting.
(B) can be used to drive a round-robin (cyclic) choice from a number of data sources, cyclically, by connecting its outputs to the control inputs of a MUX, and connecting the MUX’s data inputs to the data sources.
(C) cannot be parallel-loaded if it is based on toggling (JK) flip-flops.
(D) must be reset to 0 when if reaches its maximum value (or reset to its maximum value when it reaches 0, in the case of a down-counter).

7 Shift-registers…
(A) can be used for multiplication, but not division, by powers of 2.
(B) can be used for parallel-to-serial and serial-to-parallel conversion.
(C) are used to move information to the correct location in a Random-access memory.
(D) store the status of the shift key on a computer keyboard, but the name shift key is misleading, because they also store the status of caps-lock, and the other control keys.

8 Tri-state logic…
(A) was invented virtually simultaneously by researchers in California, Massachusetts and Washington (the state). Hence the name.
(B) only allows a chip to drive its output to the power supply voltage when output-enable is true.
(C) cannot be used with bus-based architectures, because of voltage conflicts on the shared data paths.
(D) was invented virtually simultaneously by researchers in California, Massachusetts and Alabama. Hence the name.

9 In a properly designed ASM…
(A) conditional outputs are optional, conditional tests are optional, but at least one unconditional output must be made true in each state.
(B) there are no states with no outputs.
(C) all states should have a conditional test to ensure that the state following the current state is correct.
(D) successive states happen on successive clock pulses, but the ASM can occupy a single state for long periods of time.

10 A computer processor…
(A) generally divides data processing tasks amongst a number of independent units.
(B) generally integrates control and data processing in a single monolithic unit.
(C) uses a special register, capable of being incremented and parallel-loaded, called the Program Counter, to specify the next memory address which will be accessed.
(D) is specifically designed to support a particular instruction set, and must be redesigned from scratch if any alterations in the instruction set are made.

[1]
11 The stack in the 8051 processor is…
(A) necessary for subroutine calls and interrupts.
(B) able to be disabled only during interrupt routines
(C) provides indexed offset addressing for subroutine parameters
(D) located in code memory

12 The braces in the programming language C (eg. if (A>B) { ... }) are used to group statements. In assembler the equivalent construct…
(A) is needed but only when using the simulator, the real processor doesn’t need them.
(B) isn’t needed.
(C) is the ORG – END construct.
(D) is always implemented with conditional jumps (eg JZ, JNZ …).

13 In many processors, local variables and parameters are usually stored on the stack. This is not normally done with the 8051 processor. Why not?
(A) The memory space available to the stack is very small and often needed for other purposes.
(B) The stack is located in external data ram and access to it via dptr is too slow.
(C) The assembler doesn’t have arrays and records so there is no need for local variables.
(D) The stack is only needed for interrupts or when switching register banks.

14 If the routine OUTCH is available and displays the ASCII character corresponding to the value contained in the accumulator, what is displayed by the OUTCH call in the following code?

```assembly
mov r2, #2
mov r0, #’A’
loop:
    inc r0
    djnz r2, loop
mov a, r0
lcall OUTCH
```

(A) C
(B) r0
(C) A
(D) none of the above

15 The sbuf register is sometimes critical to the correct functioning of a program. This would be when:
(A) the single bit underflow flag is used instead of the carry bit.
(B) it is necessary to move segments of memory between data and code memory.
(C) the program uses the global string buffer.
(D) serial I/O routines are used.

16 What does the instruction mov 17, @r0 do?
(A) moves the contents of the memory location pointed at by r0 to memory location 17.
(B) moves the data value 17 to the memory location pointed at by r0.
(C) moves the value in r0 to memory location 17.
(D) moves the contents of memory location 17 to the memory location pointed at by r0.
The EQU directive when used in assembler code…
(A) should be avoided if possible. The extra code for the equivalence test decreases readability.
(B) is intended to provide a means of determining equality between two byte values.
(C) is intended to provide a means of providing a textual equivalent to a value or label.
(D) is intended to provide a means of defining the actual memory location used to hold the next instruction.

The 8051 does not have many relational comparison instructions. This is…
(A) an advantage as these aren’t needed when you have both internal and external data RAM.
(B) only an advantage when using shift and rotate instructions together with a mask.
(C) a disadvantage as it complicates comparisons.
(D) only a disadvantage when interrupts are used.

The additional register banks (RB1-3) in the 8051…
(A) should be avoided – Register bank 0 is in internal RAM whereas the others are in external RAM and are therefore slower.
(B) are controlled by direct input from I/O pins on the processor.
(C) are only to be used by interrupt routines.
(D) are accessed via status bits in the PSW.

Which of the following statements is true about block parity checks?
(A) They can be sure to detect at most one error in a block.
(B) They can be sure to correct up to two errors in a block.
(C) They can be sure to detect up to four errors in a block.
(D) They can be sure to detect up to three errors in a block.

When using the HLDC protocol in ARM mode (Asynchronous Receive Mode) which of the following statements is true?
(A) The secondary machine may not transmit until it is polled.
(B) Every frame transmitted must be acknowledged.
(C) Either machine can initiate transmission.
(D) Data frames are not numbered.

Which of the following is true of fibre optics?
(A) An optic fibre has a much higher bandwidth than a coaxial cable.
(B) Signals carried by optical fibres are degraded by external electromagnetic fields.
(C) An optic fibre must be at least 1mm thick.
(D) An optic fibre is normally used to carry signals in both directions at the same time.

QAM is a method of signal modulation. Which of the following statements is true?
(A) QAM is used by a computer to communicate with a modem.
(B) QAM combines amplitude and frequency modulation.
(C) QAM is used by the parallel port on a PC.
(D) QAM combines phase and amplitude modulation.
24 In HLDC (High-level Data Link Control) which of the following statements is true?
(A) Each data frame starts and ends with a SYNC character.
(B) Each data frame starts and ends with the binary pattern 01111110.
(C) Bit stuffing is used as an aid to error correction.
(D) An 'accidental' ETX character in the data must be preceded by a DLE character.

25 Which of the following statements is true of CRC (cyclic redundancy code)?
(A) CRC uses polynomial division to calculate check bits.
(B) CRC is used in Forward Error Correction.
(C) CRC is a method of calculating the Hamming distance between codes
(D) CRC calculates both horizontal and vertical check bits.

26 In the OSI model, which of the following statements is true?
(A) The Data Link layer recognizes the links in web pages.
(B) The Transport layer controls the local area networks.
(C) Electronic mail programs belong to the Application layer.
(D) The Physical layer is responsible for acknowledging the arrival of data frames.

27 Which of the following statements is true of packet switching?
(A) Packet-switching requires more memory than message-switching.
(B) With packet-switching packets may arrive at the destination in the wrong order.
(C) With packet-switching there is no limit on blocksize.
(D) Packet switching prevents data loss.

28 Which of the following statements about Manchester encoding is true?
(A) Manchester encoding is a type of error-detecting code.
(B) Manchester encoding requires twice the bandwidth of binary encoding.
(C) Manchester encoding is a type of frequency modulation.
(D) Manchester encoding transmits one byte at a time on a serial line.
Section B (long answers)

Answer questions 29 to 31 in the blue answer booklet provided

DO WRITE the numbers of the questions you have answered from this Section on the front cover of your blue answer booklet

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29  (A) Design a digital circuit that inputs a three-bit number and generates a TRUE output when the value of the number exceeds 2.

(B) Design a digital circuit that is capable of stacking two 2-bit words. It should have two control lines, PUSH and POP. When a clock edge (high-going or low-going at your preference) occurs, if PUSH is TRUE, a 2-bit word is loaded into the stack. When a clock edge (high-going or low-going at your preference) occurs, if POP is TRUE, a 2-bit word is POPped off the stack. Words are POPped in the opposite order to the order in which they are PUSHed. If POP is executed after all PUSHed values have been POPped, zero should be output.

Hints:
• This is not an ASM design exercise
• Design a steering circuit as a separate unit, and draw it as a “black box” with the appropriate inputs, as many times as necessary.

(C) Draw a block diagram of the data-processing section of the Pico-computer architecture. Describe how the following block-transfer instruction could be implemented.

MOVE BYTES SOURCE DEST

The MOVE instruction copies the data stored in the range M[SOURCE] to M[SOURCE+Bytes} to the range M[DEST] to M[DEST+BYTES].

Hints:
• You do not need to include the control lines for the components in the block diagram.
• You may find it helpful to describe the new instruction using a piece of ASM diagram, but this is not essential.
• Modify the diagram by adding two parallel-loadable counters. You should show the control lines for these components.
(A) The while loop and if-then-else constructs used in high level languages can be implemented in assembler by using templates. Describe a possible template for each of the while loop and if-then-else constructs and illustrate your answer by showing the 8051 assembler equivalents of:

```c
int k;

k = 32;
while (k > 10) {
    k = k - 1;
}

if (k < 10)
    { k = k + 1; }
else
    { k = k - 1; }
```

(B) Write a routine printhex in 8051 assembler. Its purpose is to display a single byte value as two hexadecimal characters (using the characters 0-9 and A-F). On entry to printhex, the address of the byte whose value is to be printed is in the register r0.

The routine PUTCH already exists and will print one character. The character to be printed is expected to be in the accumulator.

(C) The architecture used for the assembler section of this course is based on the 8051.

For unsigned numbers larger than 255, multiple bytes must be used to store each number. Write a subroutine in 8051 assembler to perform multi-byte subtraction.

On entry to the subroutine:
- r0 contains the address of the first byte of N1 - the first number.
- r1 contains the address of the first byte of the N2 - second number.
- r2 contains the number of bytes in each number (they’re the same).

The numbers are stored so that the least significant byte is stored at the specified memory address and any additional bytes of the number are stored in consecutive locations in ascending address order. The result is stored in the same location as N1 (i.e. the subroutine implements N1 = N1 - N2).
(A) What is the purpose of Huffman encoding, and how does it achieve its purpose?

(B) Suppose that a computer application is sending information that is coded using 6 symbols: a, b, c, d, e, f. Experience shows that these 6 symbols occur with the frequencies:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>24%</td>
</tr>
<tr>
<td>b</td>
<td>18%</td>
</tr>
<tr>
<td>c</td>
<td>29%</td>
</tr>
<tr>
<td>d</td>
<td>15%</td>
</tr>
<tr>
<td>e</td>
<td>9%</td>
</tr>
<tr>
<td>f</td>
<td>5%</td>
</tr>
</tbody>
</table>

Construct an efficient Huffman Code for these symbol frequencies and explain your method? What is the bit sequence that would be used to encode the data sequence efface?

(C) • In OSI terms, what is the difference between a protocol and an interface?
• What are TCP and IP?
• To which OSI layers do TCP and IP belong?
• When data is transferred between application programs using TCP/IP, by which layers is the file fragmented and reassembled, and which layers will do what error detection and acknowledgement?